

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

**THIS PAGE BLANK (USPTO)**

PCT

WORLD INTELLECT  
Intc.



INTERNATIONAL APPLICATION PUBLISHED

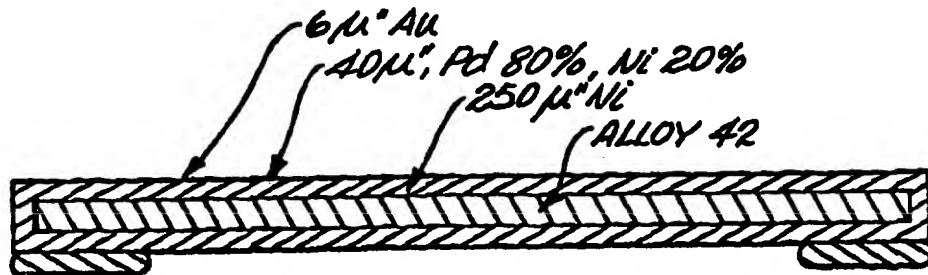
(51) International Patent Classification <sup>6</sup> : H01L 23/02, 23/04, 23/12, 21/465, H01S 4/00		A1	(11) International Publication Number: <b>WO 96/02941</b> (43) International Publication Date: 1 February 1996 (01.02.96)
(21) International Application Number: PCT/US95/09124 (22) International Filing Date: 19 July 1995 (19.07.95) (30) Priority Data: 08/277,145 19 July 1994 (19.07.94) US (71) Applicant: JOHNSON MATTHEY ELECTRONICS, INC. [US/US]; East 15128 Euclid Avenue, Spokane, WA 99216 (US). (72) Inventor: LI, Jianxing; North 4908 Calvin Road, Spokane, WA 99216 (US). (74) Agent: GIOIA, Vincent, G.; Christie, Parker & Hale, P.O. Box 7068, Pasadena, CA 91109-7068 (US).			(81) Designated States: BR, CA, DE, JP, KR, MX.  Published With international search report.

(54) Title: METAL COVER FOR CERAMIC PACKAGE AND METHOD OF MAKING SAME

(57) Abstract

A solderable metallic cover for hermetically sealing a ceramic package that includes an iron or iron-alloy core and layers of nickel or nickel alloy on the core and palladium or palladium alloy on the nickel layer.

*EXAMPLE OF NEW LID*



**METAL COVER FOR CERAMIC PACKAGE  
AND METHOD OF MAKING SAME**

**Background of the Invention**

5 This invention relates to a sealing cover which is particularly suitable for sealing ceramic packages for semiconductor devices, and to a method of producing the same.

The use of ceramic packages for semiconductor devices is well-known. Typically, such a package includes a ceramic container to which the cover must be sealed. Sealing covers, also known as "lids," of the type used in connection with containers for  
10 semiconductor devices are well known and typically include one or more layers of gold, often of substantial thickness, to aid in corrosion resistance as well as to provide for electrical connection of leads. Such covers are not only expensive, but also introduce a possible health hazard since cyanide solutions are often used in gold plating.

The present invention is directed to a novel sealing cover, and to a method of making  
15 same, which avoids or at least substantially reduces the use of gold, thus lowering cost and reducing potential health hazards by eliminating or greatly minimizing gold plating. By eliminating or minimizing use of gold, material and manufacturing costs related to the production of lids for semiconductor packages can be significantly lowered. In accordance with the present invention, a sealing cover is provided which is not only economical because  
20 it replaces gold with palladium, but is also of sufficiently high quality to pass standard tests for temperature cycling and thermal shock as well as resistance to corrosion in a salt atmosphere.

Although use of palladium in the manufacture of sealing covers is known, such use has been primarily limited to palladium in the form of palladium-silver paste applied to  
25 ceramic lids. This use merely takes advantage of the ability of palladium to fuse to ceramic in paste form. However, even in such uses only small quantities of palladium paste are employed, generally around the perimeter of the cover, and the use of palladium in this manner does not materially reduce or affect the overall manufacturing costs.

Miyoshi, et al. U.S. Patent No. 4,640,436 has suggested the use of a coating of gold,  
30 palladium, silver or platinum on a solder ring to assist in diffusion bonding of the solder to the lid. In this case, the lid is plated with "a material of high solderability" such as gold. In Levine U.S. Patent Nos. 4,835,067 and 4,666,796, it is suggested to use palladium as a solderable coating on a metal lid as two distinct layers of palladium with a layer of a more reactive metal sandwiched between the two palladium layers. Patentee provides this structure  
35 to cancel the galvanic effect that the noble top layer would normally have on the iron-based substrate to which the layers are applied to avoid a possible "short circuit" created if the iron and gold become connected through pinholes in an intermediate layer.

The present invention differs from the prior art, and in particular the disclosures in

1     Detailed Description of the Invention

      In the sealing cover construction described in FIG. 1, the final layer consists of a substantially thick layer of gold. If it is possible to reduce the thickness of the gold coating or eliminate it altogether, while retaining the required characteristics of corrosion resistance, etc. a significant reduction in manufacturing costs would occur. This is accomplished by the cover described in FIG. 2, which is an example of the invention wherein a metallic core is coated with a nickel-containing material, but a palladium-containing layer is applied onto the nickel layer. The use of palladium or a palladium alloy in this manner avoids the need for a thick outer layer of gold and, for many applications, allows the gold layer to be omitted altogether. The term "palladium alloy" as used herein refers to an alloy in which palladium is a major constituent and present in an amount of at least about 30 wt. %.

      In accordance with the presently preferred embodiment of the invention, a suitable metallic core, such as one made of iron-nickel alloy, known as "Alloy 42," "Alloy 45" or "Alloy 46" or the alloy known as "Kovar," may be provided. Alloys 42, 45 and 46 refer to compositions containing 42, 45 and 46 wt. % nickel, respectively. The particular composition of the core is not critical to the success of the cover of the invention and any iron-based alloy may be used for this purpose provided similar thermal expansion characteristics to ceramic is maintained.

      A first layer of nickel or nickel alloy is applied to the core. The nickel-containing material may be applied as an electrolytic or "electroless" coating. Presently, an electrolytic nickel-containing coating is preferred, because it appears to provide good corrosion resistance and economical and repeatable manufacture process. In lieu of a nickel or nickel alloy, a first layer of tin, silver, cadmium, indium, lead, copper, cobalt, ruthenium, iridium, zinc, or their alloys, may be employed. However, it has been determined that nickel and nickel alloys are preferred for their combination of cost, relative ease of application and resistance to corrosion.

      The thickness of the first layer is very important in producing a sealing cover with desirable properties. It has been determined that the thickness of the nickel/nickel-alloy layer should be in the range of 100 to 800  $\mu$ in. Although performance characteristics equal to that obtained with present technology can be achieved with as little as 100  $\mu$ in, a cover with superior properties is not achieved until the minimum thickness of the nickel/nickel-alloy layer is in the range of 400 to 600  $\mu$ in. The nominal thickness of this layer is advantageously about 500  $\mu$ in.

      As a second layer, it is important to use a layer of palladium or palladium alloy (as defined previously), and in particular, a palladium-nickel alloy. The most preferred composition presently is an alloy of about 80% palladium and about 20% nickel; however, alloys of at least about 30 wt. % palladium, balance nickel, silver or tin, are also particularly advantageous. In lieu of palladium and palladium alloys as aforesaid, however, it may be

1 Table 1.

TABLE I

<u>Sample I.D.</u>		<u>Metallization</u>	<u>Thickness</u>
5	A1	Matte Sulfamate Nickel	(250 $\mu$ in) Pure Gold(
	50 $\mu$ in)	A2	Matte Sulfamate Nickel (250 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
	A3	Matte Sulfamate Nickel	(250 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
10	A4	Pure Gold	( 7 $\mu$ in)
		Matte Sulfamate Nickel	(250 $\mu$ in)
	Tin/Zinc	(100 $\mu$ in)	
	B1	Electroless Nickel	(250 $\mu$ in)
	Pure Gold	( 50 $\mu$ in)	
	B2	Electroless Nickel	(250 $\mu$ in)
	Palladium/Nickel	( 50 $\mu$ in)	
	B3	Electroless Nickel	(250 $\mu$ in)
		Palladium/Nickel	( 50 $\mu$ in)
	Pure Gold	( 7 $\mu$ in)	
15	B4	Electroless Nickel	(250 $\mu$ in)
	Tin/Zinc	(100 $\mu$ in)	
	C1	Electroless Nickel	(150 $\mu$ in)
		Matte Sulfamate Nickel	(100 $\mu$ in)
	Pure Gold	( 50 $\mu$ in)	
20	C2	Electroless Nickel	(150 $\mu$ in)
		Matte Sulfamate Nickel	(100 $\mu$ in)
	Palladium/Nickel	( 50 $\mu$ in)	
	C3	Electroless Nickel	(150 $\mu$ in)
		Matte Sulfamate Nickel	(100 $\mu$ in)
	Palladium/Nickel	( 50 $\mu$ in)	
	Pure Gold	( 7 $\mu$ in)	
	C4	Electroless Nickel	(150 $\mu$ in)
		Matte Sulfamate Nickel	(100 $\mu$ in)
	Tin/Zinc	(100 $\mu$ in)	
25	D1	Semi-bright Sulfamate Ni	(125 $\mu$ in)
	Matte Sulfamate Nickel	(125 $\mu$ in)	
	Pure Gold	( 50 $\mu$ in)	
	D2	Semi-bright Sulfamate Ni	(125 $\mu$ in)
		Matt Sulfamate Nickel	(125 $\mu$ in)
Palladium/Nickel	( 50 $\mu$ in)		
30	D3	Semi-bright Sulfamate Ni	(125 $\mu$ in)
		Matte Sulfamate Nickel	(125 $\mu$ in)
	Palladium/Nickel	( 50 $\mu$ in)	
	Pure Gold	( 7 $\mu$ in)	
	D4	Semi-bright Sulfamate Ni	(125 $\mu$ in)
		Matte Sulfamate Nickel	(125 $\mu$ in)
	Tin/Zn	(100 $\mu$ in)	
	E1	Palladium/Nickel	( 10 $\mu$ in)
		Matte Sulfamate Nickel	(240 $\mu$ in)
	Pure Gold	( 50 $\mu$ in)	
35	E2	Palladium/Nickel	( 10 $\mu$ in)
		Matte Sulfamate Nickel	(140 $\mu$ in)
	Palladium Nickel 80/20	( 30 $\mu$ in)	
	E3	Palladium/Nickel	( 10 $\mu$ in)
		Matte Sulfamate Nickel	(140 $\mu$ in)

1	Solution temperature	150°F
	Current	Cathodic at 4 volts
	Exposure time	10 minutes
Step 2	<u>D.I. WATER RINSE</u>	
5	Exposure time	10 minutes
Step 3	<u>ACID ACTIVATOR</u>	
	Hydrochloric acid	30% by volume
	Solution temperature	Ambient
	Exposure time	10 minutes
10	Step 4	<u>D.I. WATER RINSE</u>
	Exposure time	2 minutes
Step 5	<i>Alternate A</i> <u>ELECTROLYTIC NICKEL</u>	
15	Product	Matte sulfamate nickel
	Nickel concentration	0.5 lbs/gal
	Nickel bromide	2.0 oz/gal
	Boric acid	4.0 oz/gal
	pH	4.3
	Solution temperature	130°F
	Current	12 amperes
20	Deposition Rate	90 $\mu$ in/hour
Step 5	<i>Alternate B</i> <u>MID-PHOS ELECTROLESS NICKEL</u>	
	Product	Mid-Phos electroless nickel
	Nickel concentration	0.5 lbs/gal
25	pH	5.0
	Solution temperature	150°F
	Deposition Rate	350 $\mu$ in/hour
Step 6	<u>D.I. WATER RINSE</u>	
	Exposure time	2 minutes
30	Step 7	<u>ACID ACTIVATOR</u>
	Hydrochloric acid	30% by volume
	Solution temperature	Ambient
	Exposure time	10 minutes
Step 8	<u>D.I. WATER RINSE</u>	
35	Exposure time	1 minute
Step 9	<u>PALLADIUM/NICKEL ALLOY</u>	
	Product	80% Pd - 20% Ni

1 relatively low melting-point solders are additionally preferred so as to avoid the necessity of  
exposing the semiconductor device within the package to elevated temperatures, such as  
might possibly injure the semiconductor. Solder compositions include solders containing in  
wt. % about 75% tin, about 20% silver and about 5% antimony; solders containing about  
5 84.5% lead, 5.5% indium, 5% tin, 3% antimony and 2% silver; and solders containing up  
to about 95% lead, preferably not less than 90% lead, up to about 5% palladium and which  
may additionally include up to about 5% silver, up to about 5% bismuth, up to about 5%  
antimony, and up to about 5% gold or a mixture of gold and tin having up to about 5% gold  
and up to about 2% tin. Other useful solders include 95% Pb-5% Pt.

10 Preferred solder compositions include Pb + Pd (Pd = 2-10 wt. %) and Pb + Pt (Pt  
= 2-10 wt %), with the following additional elements:

Ag = 0-30 wt. %

Au, Sb, Bi, In, Sn = 0-10 wt. %,

15 in solders with a melting point of about 220-310°C. Such solders exhibit controlled wet/flow  
characteristics when reflowed on the covers described herein and demonstrate good visual  
quality and reliability of sealed packages. Examples of preferred solder compositions include  
Pb + 4.75% Pd + 5% Ag; and Pb + 5% Pd + 15% Ag.

20 To further illustrate solders useful in accordance with the present invention, 12 solder  
compositions shown in the following table have been prepared:

25

30

35



1 extrusion pressure = 2000-3000PSI, extrusion rate = 20-100IPM.

Strip roll

5 Preheat 350-450F for 30 minutes, rough roll at 350-450F with reduction of over 0.020" to thickness of 0.010", finish roll at 200-300F with reduction of 0.001-0.004" to thickness of 0.002-0.005", rolling lubricant = 4-B oil or Hexane.

Strip clean

10 Methylene chloride bath clean followed by inert gas bagging to prevent oxidation of the pb solder.

Perform punch

Die punch into specified preforms.

15 Preform clean

Methylene chloride bath clean followed by inert gas bagging to prevent oxidation of the pb solder.

Preform tack weld to cover

20 Tack weld the preform to the cover (made from a conductive substrate and plated with a solderable surface layer) to form a preform/cover assembly.

Package cover/preform assembly

25 Put the preform/cover assemblies into appropriate plastic packages and fill the package with an inert gas to prevent Pb solder oxidation during shipping and storage.

Method B. Continuous cast

30 Alloy and continuous slab cast

Make appropriate alloy and form a continuous cast slab of about 0.200" thick and 2.500" wide under inert gas protection with cooling water to reduce the alloy segregation and obtain fine crystal structure.

35 Strip roll

Same procedure as in Method A.

Strip clean

1 alloy and 5  $\mu$ in Au results in < 0.5% surface area corrosion and an average of about 0.1%.

The following is an example of one preferred embodiment. A core of "Alloy 42" is spot welded to a solder ring, i.e., preform. Three steps are used to fabricate a complete lid.

- 5 A. Plated lid production.  
B. Solder ring production and punching.  
C. Attachment of the solder ring to the plated lid.

Each process is described in detail below.

#### A. Plated Lid Production

10 Alloy 42 (Fe 58%, Ni 42%) is rolled into sheets 0.010" to 0.015" thick, and annealed into a state making it suitable for punching (typically 95,000 psi tensile strength). The sheet is slit into coils wide enough to make them easily punched through a progressive die set.

Using standard technology this material is then punched into sizes suitable for sealing onto ceramic packages. Typical sizes include:

- 15
- |         |         |        |
|---------|---------|--------|
| .250" x | .375" x | 0.010" |
| .505" x | .505" x | 0.010" |
| .860" x | .860" x | 0.015" |

20 The punched squares may then be deburred chemically or mechanically to clean up any rough edges that may result from metal shearing.

The cleaned and deburred lids may then be loaded into a plating barrel for degreasing, oxide removal, and electroplating of all desired layers. One barrel of low cost lids were plated using the following sequence:

25 1. A Sterling System 6" x 12" plating barrel was loaded about 30% full with .605" x .605" x 0.010" alloy 42 squares which had been previously punched and deburred in the manner described above.

2. This barrel was plated with nickel, palladiumnickel and gold using the following sequence:

- 30 a. Electroclean at 5 volts anodic for 5 minutes;  
b. Rinse for at least 5 minutes;  
c. Descale in acid blend for 5 minutes;  
d. Rinse for 2 minutes;  
e. Plate in Sulfamate Nickel for ample time to deposit 500  $\mu$ in;  
f. Rinse for 5 minutes;  
35 g. Acid activate in 5% HCl (optional);  
h. Plate in Pd-Ni for ample time to deposit 40  $\mu$ in;  
i. Rinse for 5 minutes;  
j. Plate in a high adhesion pure gold bath for ample time to deposit 5  $\mu$ in

## 1 WHAT IS CLAIMED IS:

5 1. A solderable metallic cover for hermetically sealing a package containing a semiconductor device comprising a core of iron or iron-nickel alloy, a first layer on said core comprising nickel, tin, silver, cadmium, indium, lead, copper, cobalt, ruthenium, iridium, zinc, and alloys thereof, and a second layer on said first layer comprising palladium, tin, platinum, silver, cadmium, indium, cobalt, lead, rhodium, ruthenium, iridium, and alloys thereof, and a layer of gold on said second layer of a thickness of 0 to 50  $\mu\text{in}$ .

10 2. A cover according to claim 1 wherein said first layer comprises one from the group consisting of electrolytic and electroless nickel and alloys of nickel of a thickness of 100 to 800  $\mu\text{in}$ .

15 3. A cover according to claim 2 wherein said first layer is 400 to 600  $\mu\text{in}$ .

4. A cover according to claim 1 wherein said second layer comprises 20 to 60  $\mu\text{in}$ .

20 5. A method of assembling a semiconductor device package comprising soldering a cover according to claim 1 to a ceramic enclosure having a semiconductor device therein to hermetically seal said package with a gold-free solder selected from the group consisting of solders containing at least one of Pb, Sn, Ag, In, Bi, Pd, Pt and Sb, and which has a melting point in the range of from about 220°C to 300°C.

25 6. A method according to claim 5 wherein said solder comprises in wt. % about 75% Sn, about 20% Ag and about 5% Sb.

30 7. A method according to claim 5 wherein said solder comprises in wt. % about 84.5% Pb, about 5.5% In, about 5% Sn, about 3% Sb and about 2% Ag.

8. A method according to claim 5 wherein said solder comprises about 95% Pb and about 5% Pd.

35 9. A method according to claim 5 wherein said solder comprises up to about 95% Pb, up to about 5% Pd, up to about 5% Ag, up to about 5% Bi, up to about 5% Sb, up to 5% AU, and up to 7% of a mixture of Au and Sn having up to about 5% Au and up to 2% Sn.

1           17. A soldered, hermetically sealed semiconductor package comprising a ceramic  
enclosure having a semiconductor device therein and a cover soldered to the ceramic  
enclosure to hermetically seal said ceramic enclosure, said cover including a core comprising  
an iron or iron-nickel alloy, a first layer on said substrate comprising nickel, tin, silver,  
5   cadmium, indium, lead, copper, cobalt, ruthenium, iridium, zinc, and alloys thereof, a  
second layer on said first layer comprising palladium, tin, platinum, silver, cadmium,  
indium, cobalt, lead, rhodium, ruthenium, iridium, and alloys thereof, said cover being  
soldered to said ceramic enclosure with a gold-free solder selected from the group consisting  
of solders containing at least one of Pb, Sn, Ab, In, Bi, Pd, Pt and Sb, and which has a  
10   melting point in the range of from about 220°C to 300°C.

          18. A sealing cover consisting essentially of an iron and nickel alloy core, a 400  
μin thick first layer of material from the group consisting of nickel, tin, silver, cadmium,  
indium, lead, copper, cobalt, ruthenium, iridium, zinc, and alloys thereof, a 20-60 μin  
15   second layer of a material from the group consisting of palladium, tin, platinum, silver,  
cadmium, indium, cobalt, lead, rhodium, ruthenium, iridium, and alloys thereof and a layer  
of 0 to 15 μin of gold on the second layer.

          19. A sealing cover consisting essentially of an iron and nickel alloy core, a 400  
20   μin thick first layer of material from the group consisting of nickel and nickel alloys, a 20-60  
μin second layer of a material from the group consisting of palladium and palladium-nickel  
alloys and a layer of 0 to 15 μin of gold on the second layer.

          20. A method of making a sealing cover comprising providing a core of an alloy  
25   of iron and nickel, applying a first layer to the core comprising nickel or nickel alloy of 100  
to 800 μin thickness and applying a second layer onto the first layer of palladium or  
palladium-nickel alloy of 10 to 100 μin thickness.

          21. A method according to claim 19 further comprising applying a layer of gold  
30   of 0 to 15 μin thickness onto the second layer.

          22. A method according to claim 19 wherein said first layer is applied as a layer  
of 400 to 600 μin thickness.

35           23. A method according to claim 19 wherein said second layer is applied as a layer  
of 20 to 60 μin thickness.

          24. A method according to claim 19 wherein said first layer is electrolytic nickel.

- 1           34.    An assembly according to claim 26 wherein said solder comprises up to about  
10% Pd and up to about 30% Ag.

5

10

15

20

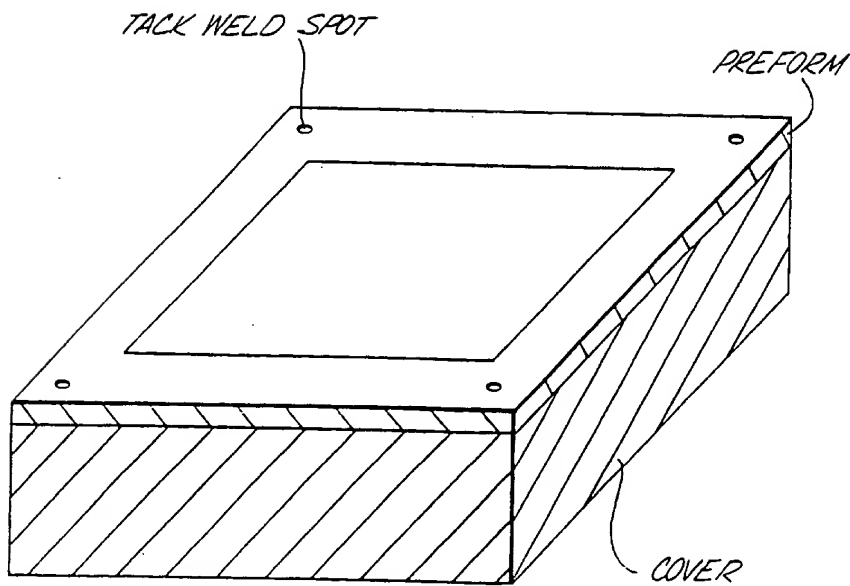
25

30

35

2/2

*Fig. 3*



## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US95/09124

## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A,4,640,436 (MIYOSHI ET AL.) 03 FEBRUARY 1987, FIGS.1-3	1-34
Y	US,A,4,601,958 (LEVINE) 22 JULY 1986, ENTIRE DOCUMENT	1-34
Y	US,A,4,331,253 (GORDON ET AL.) 25 MAY 1982, COL.3, LINES 1-49	1-34
Y	US,A,4,331,258 (GESCHWIND) 25 MAY 1982, ENTIRE DOCUMENT	1-34
Y	US,A,4,141,029 (DROMSKY) 20 FEBRUARY 1979, FIG.3	1-34
Y	JP,A, 63-5550 (YAMAWAKI) 11 JANUARY 1988, SEE CONSTITUTION	5-15,17,26-34

Form PCT/ISA/210 (continuation of second sheet)(July 1992)\*

**THIS PAGE BLANK (USPTO)**